

**IN THE CLAIMS:**

1        1. (Previously presented) A method for preventing passive release of interrupts  
2        within a computer system, the computer system having at least one processor for servicing  
3        the interrupts, one or more input/output (I/O) devices configured to issue interrupts,  
4        and an I/O bridge having a plurality of ports to which I/O devices are coupled and con-  
5        figured to interface between the I/O devices and the processor, the method comprising the  
6        steps of:

7              asserting an interrupt signal by a subject I/O device coupled to a given port of the  
8        I/O bridge;

9              forwarding an interrupt message corresponding to the interrupt signal to the pro-  
10       cessor for servicing;

11             setting an interrupt pending flag in response to assertion of the interrupt signal;

12             in response to the interrupt being serviced, generating a first ordered message, the  
13       first ordered message notifying the subject I/O device that the interrupt has been serviced;

14             generating a second ordered message for clearing the interrupt pending flag;

15             sending the first ordered message to the given port of the I/O bridge;

16             sending the second ordered message to the given port of the I/O bridge after the  
17       first message has been sent;

18             deasserting the interrupt signal in response to the first message; and

19             clearing the interrupt pending flag in response to the second ordered message.

1        2. (Original) The method of claim 1 further comprising the step of forwarding the  
2        first ordered message from the given I/O bridge port to the subject I/O device.

1       3. (Original) The method of claim 2 wherein the step of deasserting the interrupt  
2 signal is performed by the subject I/O device following its receipt of the first ordered  
3 message.

1       4. (Previously presented) The method of claim 3 wherein one of the ports of the  
2 I/O bridge is an interrupt port and the interrupt pending flag is disposed at the interrupt  
3 port, the method further comprising the step of forwarding the second ordered message  
4 from the given I/O bridge port to the interrupt port.

1       5. (Original) The method of claim 4 wherein  
2           the interrupt pending flag is implemented through a register of the interrupt port;  
3           and  
4           the second ordered message is a write transaction to the register for clearing the  
5           interrupt pending flag.

1       6. (Original) The method of claim 5 further comprising the steps of:  
2           periodically collecting a set of information regarding the assertion of interrupt  
3           signals by I/O devices; and  
4           after the step of clearing the interrupt pending flag, waiting a predetermined time  
5           before collecting a next set of information regarding the assertion of interrupt signals.

1       7. (Original) The method of claim 6 wherein the step of periodically collecting is  
2           performed through one or more serial data transfer operations.

1       8. (Original) The method of claim 1 wherein the steps of generating the first and  
2           second ordered messages are performed by the processor.

1       9. (Original) The method of claim 8 wherein the computer system includes (1) a  
2           plurality of processors at least one of which is designated to service interrupts from the

3 subject I/O device, and (2) a plurality of I/O bridges each I/O bridge coupled to a plural-  
4 ity of I/O devices configured to assert respective interrupt signals.

1 10. (Not entered)

1 11. (Original) The method of claim 1 wherein the interrupt signals are level sensi-  
2 tive interrupts (LSIs).

1 12. (Previously presented) A computer system comprising:  
2 a plurality of input/output (I/O) devices configured to assert and deassert respec-  
3 tive interrupt signals;

4 at least one processor for servicing interrupts from the I/O devices; and  
5 an I/O bridge configured to interface between the I/O devices and the at least one  
6 processor, the I/O bridge having a plurality of ports to which the I/O devices are coupled  
7 and an interrupt controller configured to detect the assertion and deassertion of the inter-  
8 rupt signals, wherein

9 the interrupt controller, in response to assertion of an interrupt signal by a subject  
10 I/O device coupled to a given port of the I/O bridge, issues an interrupt message to the at  
11 least one processor and sets an interrupt pending flag;

12 the at least one processor, upon servicing the interrupt, sends first and second or-  
13 dered messages to the given port of the I/O bridge, the first ordered message notifying the  
14 subject I/O device that the interrupt has been serviced, and the second ordered message  
15 clearing the interrupt pending flag;

16 the subject I/O device deasserts the interrupt signal in response to the first mes-  
17 sage; and

18 the interrupt pending flag is cleared in response to the second ordered message.

1 13. (Previously presented) The computer system of claim 12 wherein

2        one of the ports of the I/O bridge is an interrupt port at which the interrupt con-  
3        troller is disposed, and

4            the given port of the I/O bridge forwards the second ordered message to the inter-  
5        rupt port after forwarding the first ordered message to the subject I/O device.

1        14. (Original) The computer system of claim 13 wherein the interrupt port of the  
2        I/O bridge includes at least one register at which the interrupt pending flag is imple-  
3        mented.

1        15. (Original) The computer system of claim 12 wherein  
2            the I/O bridge port includes a read cache for buffering messages received from the  
3        at least one processor, and an ordering engine operatively coupled to a read cache, and  
4            the ordering engine is configured to release ordered messages buffered in the read  
5        cache in the same order as which they were received.

1        16. (Previously presented) The computer system of claim 12 further comprising  
2        an interrupt collector having a parallel-load shift register for receiving the interrupt sig-  
3        nals from the I/O devices, the parallel-load shift register configured to transfer informa-  
4        tion indicating the assertion or deassertion of interrupt signals to the interrupt controller  
5        through one or more serial shift operations.

1        17. (Original) The computer system of claim 16 wherein  
2            the interrupt collector transfers the information in response to a request from the  
3        interrupt controller, and  
4            the interrupt controller is configured to limit the number of serial shift operations  
5        performed by the interrupt collector so as to receive only information associated with in-  
6        terrupt signals that have been enabled.

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- 1        18. (Original) The computer system of claim 12 wherein the interrupt signals are
- 2        level sensitive interrupts (LSIs).